IN THE CLAIMS

Please amend independent claims 1, 8, 15 and 23. Please cancel claims 7, 14, 22 and 30. The text of all pending claims, along with their current status, is set forth below. This listing will replace all prior listings of claims.

1. (Currently Amended) A memory device comprising:

a capacitor having an upper cell plate and a lower cell plate;

an access transistor coupled directly to the lower cell plate of the capacitor through a first conductive plug; and

a transistor, wherein the gate of the transistor is coupled directly to the lower cell plate of the capacitor through a second conductive plug, and wherein the closest outer edge of the first conductive plug is separated from the closest outer edge of the second conductive plug by a distance in the range of approximately 20nm to 50nm.

2. (Original) The memory device, as set forth in claim 1, wherein the memory device comprises a content addressable memory device.

3. (Original) The memory device, as set forth in claim 1, wherein the lower cell plate has a surface area of approximately 100nm x 300nm.

4. (Original) The memory device, as set forth in claim 1, wherein the first conductive plug comprises a polysilicon plug.

5. (Original) The memory device, as set forth in claim 1, wherein the second conductive plug comprises a metal plug.

6. (Original) The memory device, as set forth in claim 1, wherein the second conductive plug comprises a tungsten plug.

7. (Canceled)

8. (Currently Amended) A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a capacitor having an upper cell plate and a lower cell plate;

an access transistor coupled directly to the lower cell plate of the capacitor through a first conductive plug; and

a transistor, wherein the gate of the transistor is coupled directly to the lower cell plate of the capacitor through a second conductive plug, wherein the closest outer edge of the first conductive plug is separated from the closest outer edge of the second conductive plug by a distance in the range of approximately 20nm to 50nm.

9. (Original) The system, as set forth in claim 8, wherein the memory device comprises a content addressable memory device.

10. (Original) The system, as set forth in claim 8, wherein the lower cell plate has a surface area of approximately 100nm x 300nm.

11. (Original) The system, as set forth in claim 8, wherein the first conductive plug comprises a polysilicon plug.

12. (Original) The system, as set forth in claim 8, wherein the second conductive plug comprises a metal plug.

13. (Original) The system, as set forth in claim 8, wherein the second conductive plug comprises a tungsten plug.

14. (Canceled)

15. (Currently Amended) A memory device comprising:

a content addressable memory portion comprising a first transistor coupled to a second transistor; and

a memory portion comprising an access transistor and a storage capacitor, wherein the storage capacitor comprises a first cell plate configured to form an access node of the memory device, wherein the source of the access transistor and the gate of the first transistor are coupled to the first cell plate of the storage capacitor, and , wherein the closest distance between the first conductive post and the

second conductive post is less than or equal to approximately 50nm at the first cell plate.

16. (Original) The memory device, as set forth in claim 15, wherein the lower first cell plate has a surface area of approximately 100nm x 300nm.

17. (Original) The memory device, as set forth in claim 15, wherein the source of the access transistor is coupled to the first cell plate by a first conductive post, and wherein the gate of the first transistor is coupled to the first cell plate by a second conductive post.

18. (Original) The memory device, as set forth in claim 17, wherein each of the first conductive post and the second conductive post comprise different types of material.

19. (Original) The memory device, as set forth in claim 17, wherein the first conductive post comprises polysilicon.

20. (Original) The memory device, as set forth in claim 17, wherein the second conductive post comprises a metal.

21. (Original) The memory device, as set forth in claim 17, wherein the second conductive post comprises tungsten.

22. (Canceled)

23. (Currently Amended) A system comprising:

a processor; and

a memory device couple to the processor and comprising:

a content addressable memory portion comprising a first transistor coupled to a second transistor; and

a memory portion comprising an access transistor and a storage capacitor, wherein the storage capacitor comprises a first cell plate configured to form an access node of the memory device, wherein the source of the access transistor and the gate of the first transistor are coupled to the first cell plate of the storage capacitor, and wherein the closest distance between the first conductive post and the second conductive post is less than or equal to approximately 50nm at the first cell plate.

24. (Original) The system, as set forth in claim 23, wherein the lower first cell plate has a surface area of approximately 100nm x 300nm.

25. (Original) The system, as set forth in claim 23, wherein the source of the access transistor is coupled to the first cell plate by a first conductive post, and wherein the gate of the first transistor is coupled to the first cell plate by a second conductive post.

26. (Original) The system, as set forth in claim 25, wherein each of the first conductive post and the second conductive post comprise different types of material.

27. (Original) The system, as set forth in claim 25, wherein the first conductive post comprises polysilicon.

28. (Original) The system, as set forth in claim 25, wherein the second conductive post comprises a metal.

29. (Original) The system, as set forth in claim 25, wherein the second conductive post comprises tungsten.

30. (Canceled)